Designed Workfunction Engineering of Double-Stacked Metal Nanocrystals for Nonvolatile Memory Application

Seong-Wan Ryu, Jong-Won Lee, Jin-Woo Han, Sungho Kim, and Yang-Kyu Choi

***Abstract*—A double-stacked nanocrystal (DSNC) flash memory is presented for improvement of both program/erase (P/E) speed and data retention time. Four combinations of nickel (Ni) and gold (Au) (Ni/Ni, Au/Au, Ni/Au, and Au/Ni) are used as charge storage DSNC materials and are compared from the perspective of memory performance. Through experimental results for P/E efficiency and retention time, the optimized energy band lineup for faster P/E and longer charge retention is presented. A combination of a deep potential well at the top and a shallow potential well at the bottom exhibits optimized performance in P/E, and this combination also shows the longest data retention characteristics.**

***Index Terms*—Au and Ni, double-stacked nanocrystal (DSNC), energy band lineup, flash memory, nanocrystal (NC), nanocrystal floating-gate memory (NFGM), nonvolatile memory (NVM), program/erase (P/E) speed, retention time.**

I. Introduction

POLYCRYSTALLINE-SILICON floating gates have been used as charge storage materials in nonvolatile memory (NVM) for the past three decades [1]. Recently, flash memory utilizing discrete charge storage nodes such as dielectric traps and nanocrystals (NCs) has been considered as a candidate to replace the conventional flash memory with a polycrystalline-silicon floating gate due to its superior scalability stemming from high dielectric defect immunity [2]–[5]. As dimensions of these memory devices are aggressively scaled, the thickness of the tunneling dielectric approaches its scaling limit. With respect to utilizing a thinner tunneling dielectric, the NC flash memory has attracted much attention, as a discrete storage node can allow further dielectric scaling without sacrificing memory properties such as endurance and data retention. Despite these advantages, the NC flash memory also has three major issues for the mass production. The first issue is to obtain well-ordered high-density NCs. Considering this issue, the controllability over the size, density, and ordering of NCs is crucial to increase the cell-to-cell uniformity in terms of the mass-producible devices. Thus, novel NC formation techniques were introduced such as thermal decomposition and polymeric self-assembly using a nanotemplate [6]–[8]. The second issue is related to metal NCs. The metal NC flash memory has an advantage for the enhanced program efficiency through the high density of energy states and asymmetrically enhanced electric field in NCs [9]. However, its contamination problem can evoke the degraded retention characteristic, and the lowered nonvolatility hinders the dielectric scaling. To address this issue, the optimization of annealing conditions, the utilization of a high-immunity insulator for metal diffusion, and the gate-last process were reported [10]–[12]. The last issue is to overcome the tradeoff between P/E efficiency and retention characteristics. One breakthrough can be to adopt high-k dielectrics as gate dielectrics [13].

This work is extended from the last issue of enhanced NVM performance such as P/E and retention characteristics simultaneously. In order to fully utilize the advantageous properties of NC flash memory, the tunneling dielectric must be extremely thinned. In this case, the retention time and P/E efficiency become important issues. Related to these issues, a multistacked NC flash memory structure was introduced in terms of the enhancement of program efficiency and retention characteristics [14]–[16]. Also, a high-workfunction (WF) metal NC can provide better retention characteristics and program efficiency. However, it has a weakness with respect to erase speed due to the increased potential barrier between the Fermi level of metal NC and the conduction band of the substrate. In order to achieve longer retention and a wider sensing window, the combination of a multistacked NC flash memory structure and WF engineering in the charge storage node via the use of various metal NCs may be a practical approach [14]–[19].

In this paper, a WF-engineered double-stacked NC (DSNC) flash memory is presented. Combinations of two metals separated by an interlayer (IL) dielectric form various potential well structures, which can influence memory properties. Higher WF (Au: 5.0 eV [17]) and lower WF (Ni: 4.5 eV [13], [17]) metal NC layers are utilized as charge storage nodes. Thus, Au forms a deeper potential well compared to Ni due to its higher WF. Using these two metal NC layers, four combinations of homometal and heterometal DSNCs (type I: Ni/Ni, type II: Au/Au, type III: Ni/Au, and type IV: Au/Ni [top NCs/bottom NCs]) are possible. As shown in Fig. 1, these four-split embedded NC flash memories were fabricated and assessed in terms of P/E efficiency and reliability. The differences in these memory characteristics are explained through a simple energy band model.

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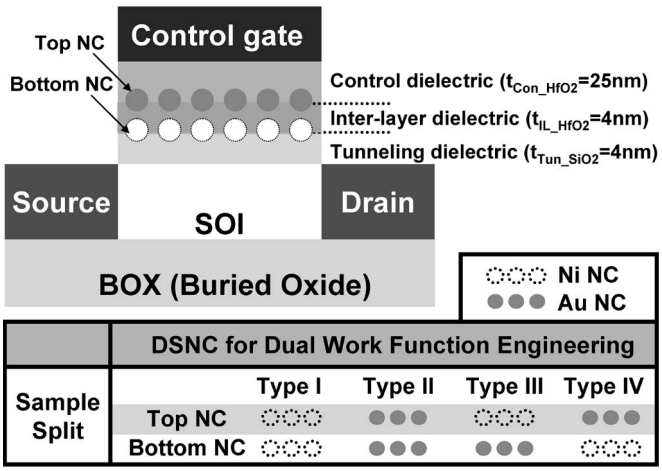

Fig. 1. Schematic of the DSNC-embedded NVM structure and four different splits: type I (Ni/NI), type II (Au/Au), type III (Ni/Au), and type IV (Au/Ni).

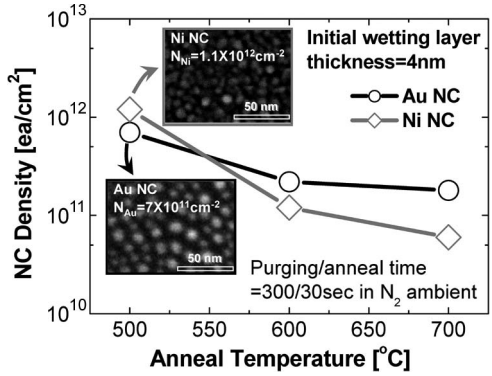

Fig. 2. NC density dependence of Ni and Au on annealing temperature with a fixed wetting layer thickness of 4 nm for both Ni and Au NCs. For Ni and Au NCs, densities of 7×10^{11} and 1.1×10^{12} cm^{-2} were achieved and chosen for the charge storage nodes in NVM DSNC devices.

The tradeoff property between P/E efficiency and retention time is analyzed and verified by comparison of the measured data and the analytically calculated tunneling probability.

II. Fabrication

The DSNC flash memory was fabricated on a p-type (100) silicon-on-insulator (SOI) substrate. The 100-nm top silicon film was thinned to 50 nm by iterative oxidation and wet-etch steps. In a metal nanocrystal floating-gate memory (NFGM) device, one important issue is melting of the metal and metal-induced contamination during high-temperature source/drain (S/D) annealing. To circumvent related problems, a gate-last process was applied. Thus, after defining the active region, $^{15}P^{+}$ was first implanted over the photoresist mask layer to form the S/D. After removal of the photoresist mask layer, tunneling oxide ($t_{\mathrm{Tun}} = 4$ nm) was grown by a thermal oxidation process. A 4-nm bottom metal wetting layer was then deposited and annealed and subsequently transformed to discrete NCs by thermal agglomeration. A scanning electron microscopy (SEM) image and the temperature dependence on NC diameter and density for Ni and Au are shown in Fig. 2. An IL dielectric of HfO_2 ($t_{\mathrm{IL}} = 4$ nm) was then deposited via atomic layer

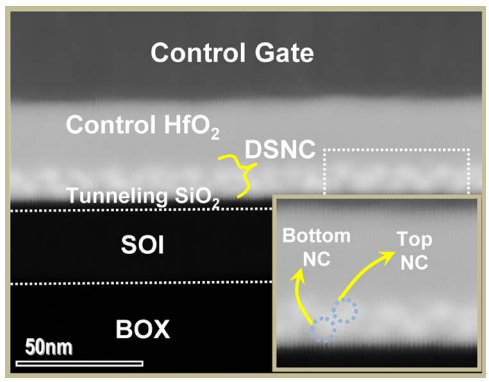

Fig. 3. Cross-sectional STEM image of a DSNC SOI NMOSFET.

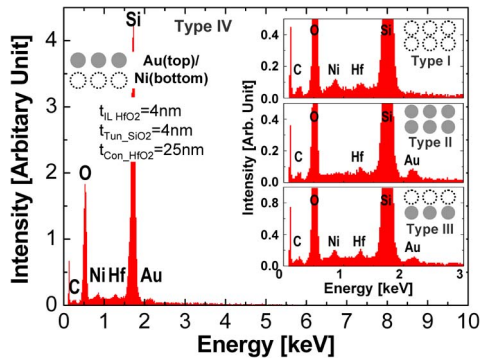

Fig. 4. EDS analysis for the Au/Ni nonvolatile DSNC device (type IV). The other types are depicted in the inset.

deposition to separate the top and bottom metal NC layers, and the upper metal NCs were formed by the aforementioned thermal agglomeration method. As a control dielectric, a 25-nm HfO_2 ($t_{\mathrm{Con}} = 25$ nm) layer was deposited, and aluminum was used as a control gate. For electrical measurement, the nominal device dimensions are 2-μm channel width and 2-μm gate length. As the temperature to induce thermal agglomeration is increased, the NC size increases, whereas the NC density decreases, as shown in Fig. 2. Because a smaller size and a larger density of the NC are desirable for NFGM applications, a 500-°C annealing temperature was chosen for the metal agglomeration step. The insets of Fig. 2 show the SEM images of the two metal NC layers. The average radii are 8 and 6 nm, and the densities are 7.0×10^{11} and 1.1×10^{12} cm^{-2} for Au and Ni, respectively. In the case of homometal (Ni/Ni and Au/Au) NC layers, two potential wells exhibit identical potential depth. In contrast, the heterometal (Ni/Au and Au/Ni) NC layers have different potential depths. This means that improvement of the NVM characteristics can be expected by carefully designing heterometal DSNCs. The cross-sectional scanning tunneling electron microscopy (STEM) image of a fabricated DSNC SOI NMOSFET is shown in Fig. 3. The double-layered NCs separated by the HfO_2 IL are observed. Also, judging from the magnified inset of Fig. 3, thermally agglomerated top NCs are formed in the valleys amid the bottom NCs. Fig. 4 shows the results of an energy-dispersive spectroscopy (EDS) analysis for each sample of the four different structures. The results of the EDS analysis verify their DSNC structures.

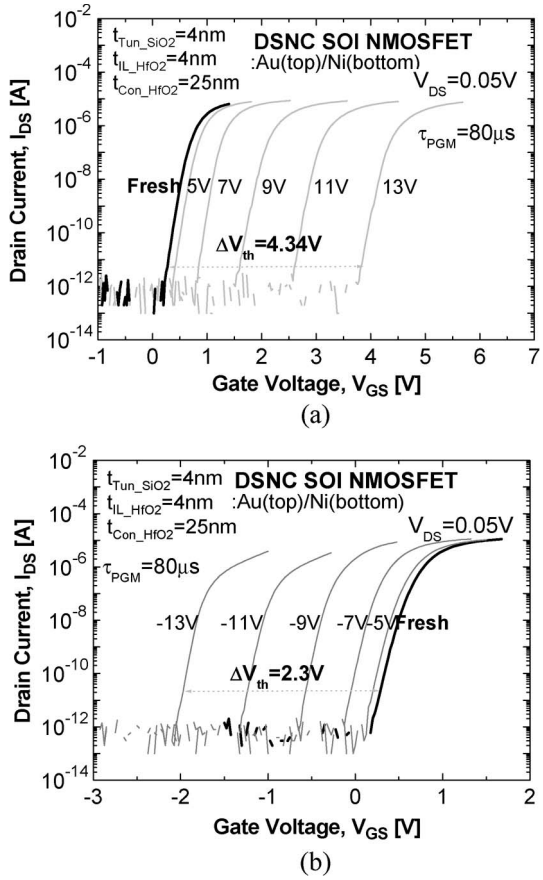

Fig. 5. Transfer characteristics for the Au/Ni sample (type IV) after (a) programming and (b) erasing by 80-μs gate pulse.

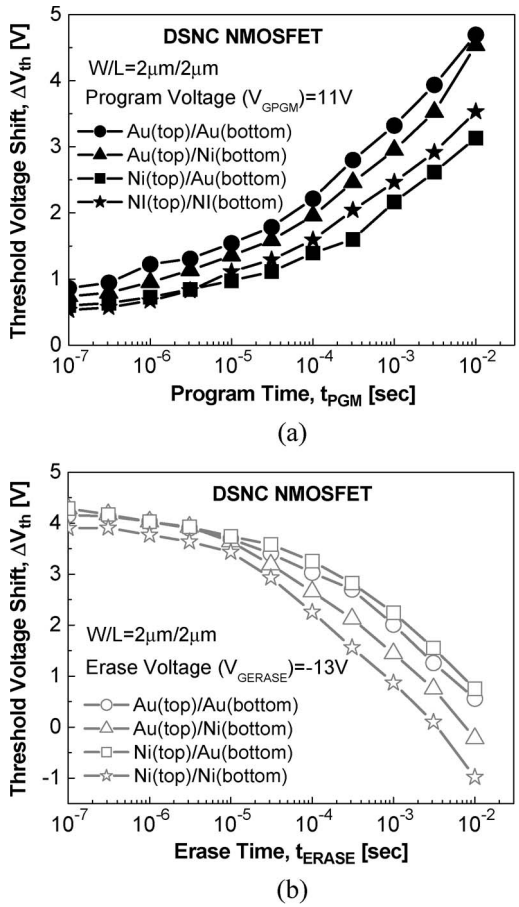

Fig. 6. Comparison of (a) program efficiency and (b) erase efficiency among the four types of nonvolatile DSNC devices.

III. Device Characteristics and Discussion

A. P/E Transient Characteristics

Data states for NC flash memory are distinguished by the existence of charges in the NC floating gate. In this paper, program/erase (P/E) was realized by a tunneling mechanism ($V_G = V_{\mathrm{GPGM}}$ or V_{GERS}, and $V_S = V_D = 0$ V with 80 μs). Fig. 5 shows the transfer characteristics of Au/Ni (type-IV) DSNC-embedded flash memory ($W/L = 2\ \mu\mathrm{m}/2\ \mu\mathrm{m}$) for P/E operations. At $V_{\mathrm{GPGM}} = 13$ V and $V_{\mathrm{GERS}} = -13$ V, the threshold voltage shift (ΔV_{th}) shows a wide memory window of 6.6 V, which is applicable to a multilevel-cell architecture. Because inherently existing traps in bulky and interfaced HfO_2 can contribute to a shift of V_{th}, the initial V_{th} shift by these traps without metal NCs should be clarified. The control device without metal NC floating gate displayed only 0.6-V hysteresis in a $\pm$11-V sweep range. Therefore, the influence of traps in HfO_2 is assumed to be negligible, and it can be concluded that DSNCs play a major role as charge storage nodes.

Fig. 6 shows the P/E transient characteristics. P/E conditions of $V_{\mathrm{GPGM}} = 11$ V for programming and $V_{\mathrm{GERS}} = -13$ V for erasing were selected. The program speed at Au (top)/Au (bottom) [type II] and Au (top)/Ni (bottom) [type IV] was shown to be faster than that at Ni (top)/Au (bottom) [type III] and Ni (top)/Ni (bottom) [type I], i.e., the program speed is ordered, from fast to slow, as follows: Au/Au $>$ Au/Ni $>$ Ni/Au $\approx$ Ni/Ni. According to [20], larger size NCs induce high program speed. As shown in Fig. 2, Au NCs are larger than Ni NCs. Thus, the better program speed at Au/Au than that at Ni/Ni can be explained by the size effect of NCs [20]. However, the size effect has difficulty in explaining the program speed difference between Au/Ni and Ni/Au. In this paper, the WF of the top metal NC more dominantly impacts the program characteristics than the size effect can do. Depending on the WF of the top NC, a fraction of charges flowing out from the top NCs through the control oxide result in charge loss, i.e., inefficient program operation. As shown in Fig. 7, when a high-WF NC layer is embedded as a top floating gate, reduced leakage and fast operation speed can be obtained [13]. In this paper, the Au NC layer showed faster speed than the Ni NC layer as a top floating gate. This means that the WF of Au NCs is expected to be higher than that of Ni NCs, although some ambiguity such as the Fermi-level pinning effects remains regarding the WFs of Ni and Au NCs, as reported in [18].

It is worthwhile to note how the program behavior depends on the bottom metal NC with Au NCs at the top. In the case of higher WF metal (Au) at the top metal NC, the tunneled charges from the channel are more easily captured in the deeper potential well than in the case of utilizing Ni as a top metal. Comparing Au/Au (type II) and Au/Ni (type IV), when a deeper potential well is formed at the bottom layer, the program speed becomes faster in type II than in type IV. However, the difference among the four types is not greatly amplified due

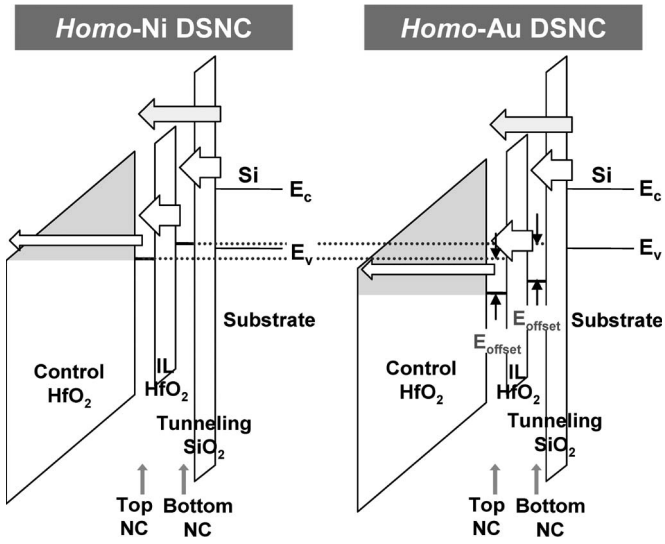

Fig. 7. Energy band diagram of control barrier/top NC/barrier by interlayer/bottom NC/tunneling barrier/substrate with positively applied gate voltage for program operation in the case of two different homometal DSNC materials of (a) Au and (b) Ni.

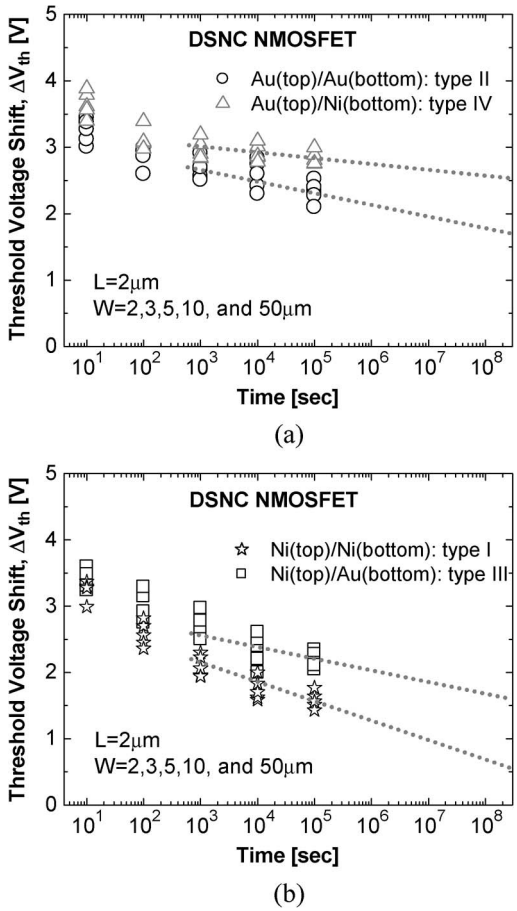

Fig. 8. Retention characteristics for the cases of (a) Au/Au (type II) and Au/Ni (type IV) and (b) Ni/Ni (type I) and Ni/Au (type III). The Au/Ni set (type IV) revealed superior charge storability due to the two-step band barrier.

to the relatively thick control HfO_2 (i.e., 25 nm). In the erase case, the erase speed is ordered, from fast to slow, as follows: Ni/Ni > Au/Ni > Au/Au > Ni/Au. This means that the bottom metal WF dominates erase behaviors, which is different from

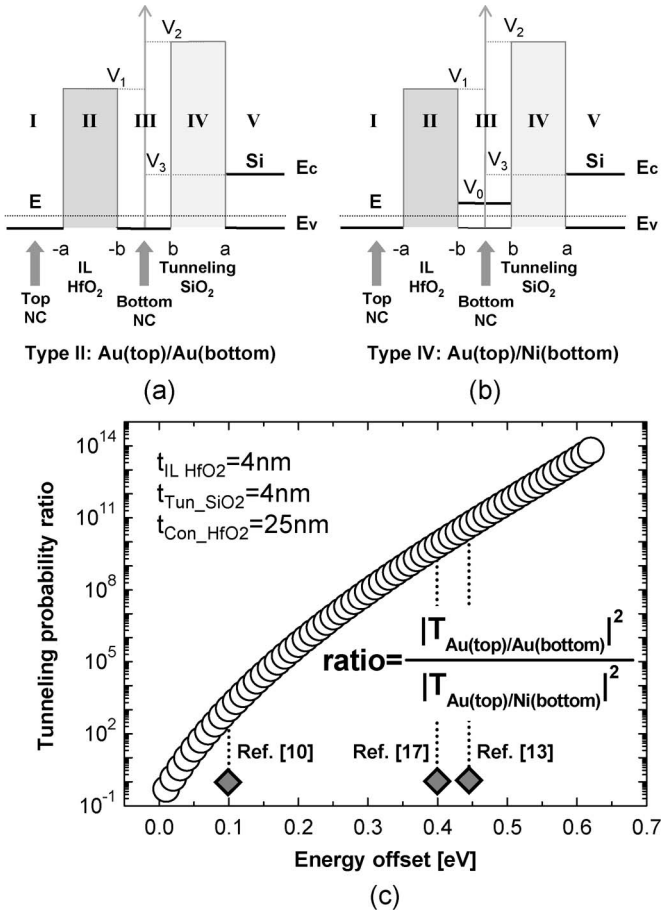

Fig. 9. Simplified energy band diagram of top NC/barrier by interlayer/bottom NC/tunneling barrier/substrate for (a) Au/Au (type II) and (b) Au/Ni (type IV) cases. (c) Calculated back-tunneling probability ratio of Au/Au to Au/Ni.

program operation due to the increased tunneling probability by the lower potential barrier of Ni NCs than that of Au NCs. As a result, a combination of higher WF at the top and lower WF at the bottom is the most optimized set (i.e., Au/Ni) in terms of fast P/E.

B. Retention Characteristics

Fig. 8 shows the data retention characteristics for the four different types. The degradation slope of the threshold voltage shift reflects the charge retention capability. Au/Ni (type IV) shows the best retention characteristics, whereas Ni/Ni (type I) exhibits the worst retention characteristics. In the case of Ni/Ni, because the top and bottom potential wells are shallow compared to other arrangements, the charge retention characteristic is the worst. In the case of Au/Ni (type IV), while the potential barrier height difference between the Ni Fermi level and conduction band of Si is small, there exists a band offset due to the difference between the top Au NC and the bottom Ni NC. Therefore, as the band offset between two metals increases, the back-tunneling probability of the stored charges at the top Au and the bottom Ni is reduced relative to the other sets.

To verify the aforementioned tendency, the back-tunneling probability from the top NC to the substrate should be compared between Au/Au (type II) and Au/Ni (type IV). Thus, the

TABLE I
TUNNELING PROBABILITY FOR THE TYPE II OF Au(TOP)/Au(BOTTOM) AND THE TYPE IV OF Au(TOP)/Ni(BOTTOM)

Tunneling probability of Au(top)/Au(bottom)
$\lvert T\rvert^2 = \dfrac{e^{-2\delta a}\{4\alpha^2k^2\cosh^2(\alpha(a-b))+(\alpha^2-k^2)^2\sinh^2(\alpha(a-b))\}}{\beta^2(\delta^2+k^2)\cosh^2(\beta(a-b))+(\beta^4+\delta^2k^2)\sinh^2(\beta(a-b))-2\beta\delta(\beta^2+k^2)\cosh(\beta(a-b))\sinh(\beta(a-b))}\dfrac{\beta^2}{\alpha^2}$
Tunneling probability of Au(top)/Ni(bottom)
$\lvert T\rvert^2 = \dfrac{e^{-(4\gamma b+2\delta a)}\{\alpha^2(\gamma^2+k^2)\cosh^2(\alpha(a-b))+(\alpha^4+\gamma^2k^2)\sinh^2(\alpha(a-b))\}-2\alpha\gamma(\alpha^2+k^2)\cosh(\alpha(a-b))\sinh(\alpha(a-b))}{\{\beta(\gamma-\delta)\cosh(\beta(a-b))+(\beta^2-\gamma\delta)\sinh(\beta(a-b))\}^2}\dfrac{\beta^2}{\alpha^2}$
$\left(\text{※}\quad \alpha^2=-\dfrac{2m(E-V_1)}{\hbar^2},\ \beta^2=-\dfrac{2m(E-V_2)}{\hbar^2},\ k^2=\dfrac{2mE}{\hbar^2},\ \gamma^2=-\dfrac{2m(E-V_0)}{\hbar^2},\ \delta^2=-\dfrac{2m(E-V_3)}{\hbar^2}\right)$

back-tunneling probability was analytically calculated with a simplified 1-D energy band diagram to show the band offset between the top and bottom NC layers, as shown in Fig. 9(a) and (b). One is a single-step energy offset [Fig. 9(a)], and the other is a double stairlike energy offset [Fig. 9(b)]. The calculated tunneling probabilities based on the Wentzel–Kramers–Brillouin approximation for Au/Ni and Au/Au are summarized in Table I. The tunneling probability was calculated as a function of the WF of the Ni NC from 4.5 to 4.9 eV due to the variation of the WF of the Ni NC [10], [13], [17], while the WF of the Au NC (5.0 eV) and the effective mass of electrons in SiO_2 and HfO_2 (SiO_2 : 0.55 m_0 and HfO_2 : 0.15 m_0 [21]) have been kept the same.

The Au/Au structure, which has single deep potential wells, provides higher tunneling probability than the Au/Ni structure, which has double stairlike potential wells, i.e., $|T_{-\mathrm{Au/Au}}|^2 \gg |T_{-\mathrm{Au/Ni}}|^2$, as shown in Fig. 9(c). However, Ni/Ni shows the poorest retention characteristics compared to other sets because of having the shallowest potential well. Therefore, the WF-designed heterometal DSNC device (Au/Ni: type IV) presents superior retention characteristics as well as P/E efficiency. This approach can be a breakthrough to overcome the tradeoff trend between prolonged retention behaviors and fast P/E.

IV. CONCLUSION

A WF-designed DSNC flash memory was demonstrated for simultaneous enhancement of both P/E efficiency and data retention time. Four combinations of nickel and gold (Ni/Ni, Au/Au, Ni/Au, and Au/Ni) were used for the top and/or bottom metal as charge storage materials and were comparatively evaluated in terms of memory performance. It was found that the top metal NC material governs the program efficiency, while the bottom metal NC material dominates the erase property. Furthermore, a deeper potential well at the top is desirable for the program efficiency, and a shallower potential well at the bottom is efficient for the erase property. Thus, the optimized set is found to be Au/Ni. In addition, the WF-designed heterometal DSNC showed superior data retention compared with the homometal DSNC. The heterometal having a lower WF at the bottom showed the best charge retention characteristic, i.e., Au/Ni was the optimal combination in terms of both retention and P/E.

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