[EE320] Digital System Laboratory

Spring 2019

- **Course Overview**
  The aim of this course is to give students hands-on experience in designing and building digital systems through practical experiments. This experimental course, related to basic circuit theory and digital systems, is focused on both hands-on experience and design practice with the following experiments: 1. Utilization of experimental equipment such as oscilloscope, power supply, and function generator, 2. Basic electric circuit theory with R, L, and C circuit networks, 3. Various digital circuits and systems, 4. Design specific digital system for given functionality as a term project.

- **Instructor**:
  - **Seong-Jin Kim**, EB3, #401-1 (kimsj@unist.ac.kr)
  - **Jongwon Lee**, EB3, #601-9 (jongwonlee@unist.ac.kr)
  - ***Team teaching*:** one professor gives lectures **every three weeks** (grade will be individually given for the two classes)

- **Office Hours**:
  - **Seong-Jin Kim**: any time by appointment
  - **Jongwon Lee**: any time by appointment

- **TA**:
  - TBD

- **Textbooks**
  - *Handouts for EE320*, ECE, UNIST
  - *Experiments in Digital Fundamentals* 10th edition, David M. Buchla, Pearson Prentice Hall.
  - *Digital Design*, 5th edition, M. Mano and M. Ciletti, Pearson Prentice Hall.
  - *Pspice User Manuals & Tutorials*

- **Grading Policy**
  - Lab session
    - 6 points per **Pre-Report** and 6 points for **Main-Report**
    - 10 points per **Lab Demonstration**
  - Term Projects
    - 40 points for **Demonstration**
    - 20 points for **Project Report**
    - 20 points for **Additional Functions**
  - Lab Total: $(6 + 10) + (6 + 6 + 10) \times 12 + (40 + 20 + 20) = 360$
  - 40 points for both **Lecture and Lab attendances**. Starting from 40 points for full attendance, -1 and -2 points for each late and absence respectively. F grade for absences more than six times.
  - Total Absolute Score: $360 + 40 = 400$

- **Requirements**
  - Pre-learning will be achieved during the lecture and the pre-report for each lab should be prepared before the lab.
  - The preliminary report should contain *Pspice* simulations for the specific circuits which

will be implemented in the lab.
  - Term projects will be achieved at the end of the lab classes during two weeks.

- **Due Dates**
  - Preliminary reports are due by the BEGINNING of the present week's lab.
  - Main reports are due by the BEGINNING of the next week's lab.

- **Lab Operation Policy**
  - If a student has a justifiable reason, he/she can change the lab section temporarily (e.g., for one week only) with permission from the involved TAs. It is recommended for the student to talk in personal to the involved TAs about the desired change at least one day in advance.
  - Written reports should be in English (exception: person's name).
  - Late reports should be submitted to the TA in charge.
  - No food or drink in the lab. Bottled water with its cap closed may be permitted. An exception to this can be made temporarily by the TA's discretion.

- **Delay Penalty**
  - One point per day (24 hours) for preliminary and main reports

- **Announcement and Homework will be given in the Blackboard**

- **Questions? (Blackboard)**
  - Please use the Web Board as much as possible. Questions directly sent by e-mail will also be OK, but it can be delayed by huge e-mails.

- **Schedule**

Week	Monday	Lab. Contents	Lab #
1	2/26	Intro: Oscilloscope, Laboratory Instrument, and Measurements of Voltage, Current, Passive Comp.	1(L)
2	3/5	BCL1: Ohm's Law and Resistive Circuits	2(L)
3	3/12	BCL2: Thevenin, Norton, Kirchhoff Theorems, and Impedance Matching	3(L)
4	3/19	BCL3: Transient Response and Resonance in RLC Circuits	4(L)
5	3/26	DLL1: Number Systems and Logic Gates	5(K)
6	4/2	DLL2: Boolean Laws, DeMorgan's Theorem, and Logic Circuit Simplification	6(K)
7	4/9	DLL3: Adder and Magnitude Comparator	7(K)
8	4/16	Midterm Exam Week	None
9	4/23	DLL4: Multiplexers and Demultiplexers	8(L)
10	4/30	DLL5: D Latch, D Flip-Flop, and JK Flip-Flop	9(L)
11	5/7	DLL6: One-Shots and Astable Multivibrators, and Asynchronous Counters	10(L)
12	5/14	DLL7: Synchronous Counters	11(K)
13	5/21	HDL1: Introduction to Hardware Description Language	12(K)
14	5/28	HDL2: Stop Watch Design	13(K)
15	6/4	TP: Implementing a Digital System using HDL	TP(K)
16	6/11	Final Exam Week	None(TP)